CLAIMS

What is claimed is:

1. A system comprising:

a first transmitter to transmit a test signal to a network;

a first receiver to receive a first signal from the network;

a second receiver to receive the test signal from the network;

a second transmitter to receive the test signal from the second receiver using a 1-bit communications line, wherein the second transmitter is to cleanup jitter in the test signal and provide the jitter cleaned-up test signal as the first signal.

2. The system of Claim 1, further comprising a data processor to provide the test signal to the first transmitter and to receive the first signal from the first receiver, wherein the first receiver is to transfer the first signal with substantially no jitter correction to the data processor as a second signal and wherein the data processor is to determine path integrity characteristics based on the test signal and second signal.

3. The system of Claim 1, wherein the first transmitter comprises:

a first clock source to provide a first clock signal based on a comparison between a second clock signal and a third clock signal;

a second clock source to provide the second clock signal based on a comparison between the third clock signal and either a fourth clock signal or an input data clock signal;

a third clock source to provide the fourth clock signal;

a phase detector to selectively provide samples of an input signal in response to the input signal and to adjust a phase of the fourth clock signal based on phase mismatches between the input signal and the fourth clock signal; and

a deserializer to convert the samples into parallel format based on the fourth clock signal.

4. The system of Claim 3, wherein the first transmitter further comprises:

a selector to selectively transfer the parallel format samples in response to loop back mode and to selectively transfer a second parallel input signal in response to transmit mode;

a de-serializer to convert the parallel format signal from the selector to serial format based on the third clock signal; and

a re-timer to provide the serial format samples from the de-serializer as the test signal based on the first clock signal.

5. The system of Claim 4, wherein the first receiver comprises:

a phase detector to selectively provide samples of the first signal as a second signal in response to the first signal and to adjust a phase of a fifth clock signal based on phase mismatches between the first signal and the fifth clock signal; and

a clock source to provide the fifth clock signal, wherein a loop bandwidth of the clock source is to transfer substantially all jitter from the first signal to the second signal.

6. The system of Claim 2, further comprising an interface to exchange signals with the data processor.

7. The system of Claim 6, wherein the interface is compatible with XAUI.

8. The system of Claim 6, wherein the interface is compatible with IEEE 1394.

9. The system of Claim 6, wherein the interface is compatible with PCI.

10. The system of Claim 6, further comprising a switch fabric coupled to the interface.

11. The system of Claim 6, further comprising a packet processor coupled to the interface.

12. The system of Claim 6, further comprising a memory device coupled to the interface.

13. The system of Claim 2, wherein the data processor is to perform media access control in compliance with IEEE 802.3.

14. The system of Claim 2, wherein the data processor is to perform optical transport network de-framing in compliance with ITU-T G.709.

15. The system of Claim 2, wherein the data processor is to perform forward error correction processing in compliance with ITU-T G.975.

16. The system of Claim 1, further comprising a data processor and wherein the first receiver is to receive the test signal from the first transmitter using a 1-bit communications line and wherein the first receiver is to transfer the test signal with substantially no jitter correction to the data processor and wherein the data processor is to determine path integrity characteristics based on the test signal.

17. The system of Claim 1, wherein the second transmitter comprises:

a first clock source to provide a first clock signal based on a comparison between a second clock signal and a third clock signal;

a second clock source to provide the second clock signal based on a comparison between the third clock signal and either a fourth clock signal or an input data clock signal;

a third clock source to provide the fourth clock signal;

a phase detector to selectively provide samples of an input signal in response to the input signal and to adjust a phase of the fourth clock signal based on phase mismatches between the input signal and the fourth clock signal; and

a deserializer to convert the samples into parallel format based on the fourth clock signal.

18. The system of Claim 17, wherein the second transmitter further comprises:

a selector to selectively transfer the parallel format samples in response to loop back mode and to selectively transfer a second parallel input signal in response to transmit mode;

a de-serializer to convert the parallel format signal from the selector to serial format based on the third clock signal; and

a re-timer to provide the serial format samples from the de-serializer as the test signal based on the first clock signal.

19. The system of Claim 18, wherein the second receiver comprises:

a phase detector to selectively provide samples of the first signal as a second signal in response to the first signal and to adjust a phase of a fifth clock signal based on phase mismatches between the first signal and the fifth clock signal; and

a clock source to provide the fifth clock signal, wherein a loop bandwidth of the clock source is to transfer substantially all jitter from the first signal to the second signal.

20. The apparatus of Claim 1, wherein the network comprises an optical network.

21. The apparatus of Claim 1, wherein the network includes a gigabit Ethernet over copper network.

22. A method comprising:

transmitting a test signal to a network;

receiving the test signal from the network;

transferring the test signal with substantially no jitter correction as a first signal using a 1-bit communications line;

substantially cleaning-up jitter in the first signal; and

providing the jitter cleaned-up first signal as a second signal to a network.

23. The method of Claim 22, further comprising determining path integrity characteristics based on the test signal and the second signal.

24. The method of Claim 22, wherein the transmitting the test signal to the network comprises:

substantially cleaning-up jitter in an input signal; and

providing the jitter cleaned-up input signal as the test signal.

25. The method of Claim 22, further comprising:

receiving the test signal using a 1-bit communications line;

transferring the test signal with substantially no jitter correction; and

determining path integrity characteristics based on the test signal transferred with substantially no jitter correction.